

Topic 2

DC Biasing of Bipolar Transistors

2.1 Introduction

The analysis or design of a transistor amplifier requires a knowledge of both the dc and the ac response of the system. Biasing a transistor is connecting passive components to the terminals of the transistor so that it operates within its limits of operation. The term biasing means the application of dc voltages to establish a desired level of current and voltage. The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. Once the desired dc current and voltage levels have been defined, a network must be constructed that will establish the desired operating point. We shall simply examine the common-emitter (CE) configuration of a BJT. The equations below can be used for biasing are:

$$V_{BE} \simeq 0.7 \text{ V} \quad (2.1)$$

$$I_C = \beta I_B \quad (2.2)$$

$$I_E = (\beta + 1) I_B \quad (2.3)$$

Fig. 2.1 shows the possible locations for an operating point. Note that the operating point can be anywhere within the region of operation, so points like B, C and D are all possible but some are better than others for reasons that will become clear later. For example, point B is a better choice than C and D because it allows for adequate current and voltage swing to the left, right, above and below it when the signal is fed into the amplifier. For the BJT to be biased in its linear or active operating region the following must be true:

- (a) The base–emitter (BE) junction must be forward-biased (B more positive than E), with a resulting forward-bias voltage V_{BE} of about 0.6 V to 0.8 V or $\simeq 0.7 \text{ V}$ (for Si BJT)
- (b) The base–collector (BC) junction must be reverse-biased (C more positive than B), with the reverse-bias voltage being any value within the maximum limits of the device.
- (c) The operating point must lie within the dashed lines in Fig. 2.1(a) and above the $I_B = 0 \mu\text{A}$ characteristic. This last condition applies only to amplification and not switching applications of a BJT.

2.1.1 CE fixed-bias BJT Amplifier

Fig. 2.2(a) is a BJT fixed-bias CE amplifier. The signal enters through capacitor C_1 and exits through C_2 after amplification. For biasing, we are only interested in DC conditions, so we consider

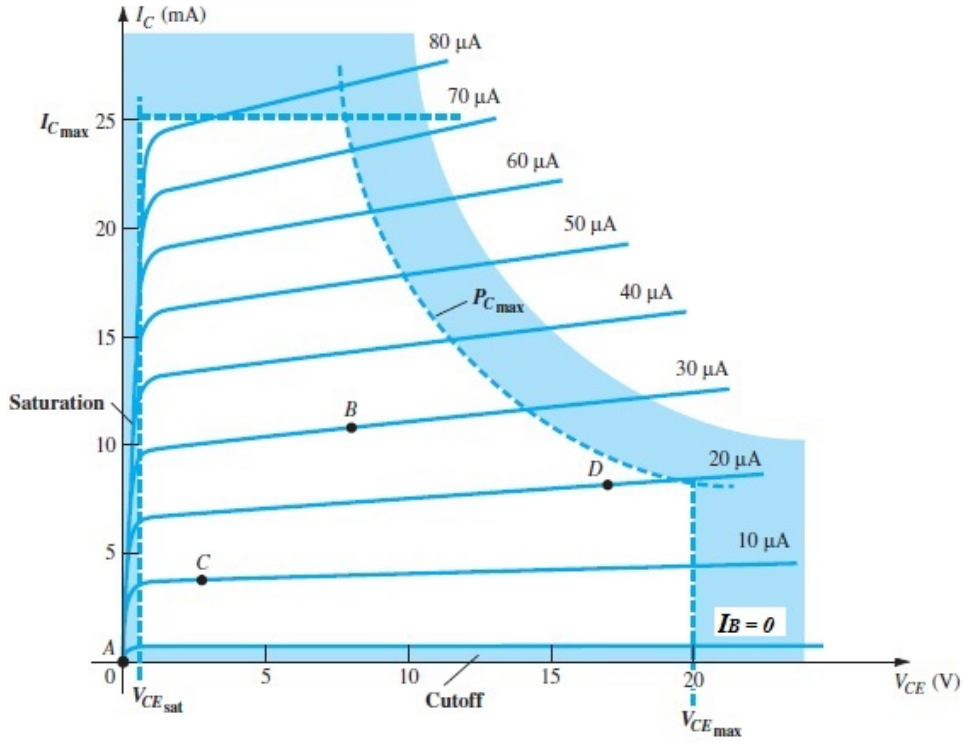


Figure 2.1: **Limits of BJT operation**

only the DC equivalent circuit shown in Fig. 2.2(b). The operating point is specified by three parameters - the base current I_B , the collector current I_C and the collector-emitter voltage, V_{CE} - these are normally further subscripted using Q as I_{BQ} , I_{CQ} , V_{CEQ} where Q stands for the Q-point (quiescent point or operating point).

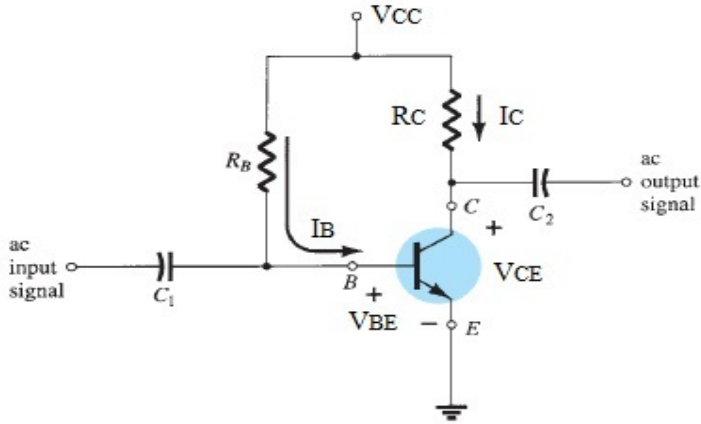


Fig. 3.2 (a) Fixed-bias CE amplifier

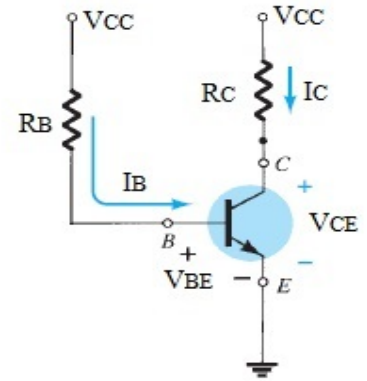


Fig. 3.2 (b) DC equivalent circuit

We apply Kirchoff's voltage law at the input side of the amplifier in Fig. 2.2(c):

$$V_{CC} = I_B R_B + V_{BE}$$

The base current I_B is given by

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} \quad (2.4)$$

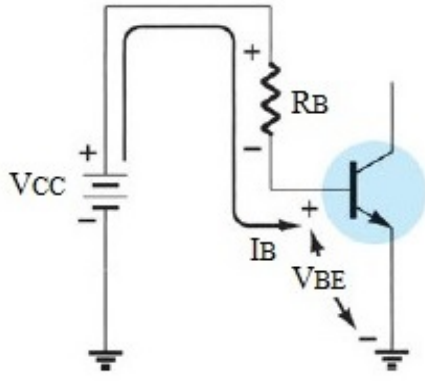


Fig 3.2 (c) Analysing input side

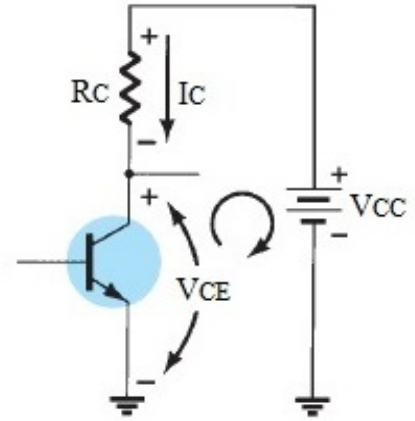


Fig 3.2 (d) Analysing output side

Figure 2.2: Fixed-bias BJT analysis

For the output side, using Fig. 2.2(d):

$$V_{CC} = I_C R_C + V_{CE}$$

and the collector emitter voltage is

$$V_{CEQ} = V_{CC} - I_{CQ} R_C \quad (2.5)$$

Using Eqn. 1.6, i.e. $I_C = \beta I_B$, we get

$$I_{CQ} = \beta I_{BQ} \quad (2.6)$$

Equation (2.5) may also be written as

$$V_{CEQ} = V_{CC} - \beta I_{BQ} R_C \quad (2.7)$$

This establishes the operating point for this fixed-bias amplifier. The Q-point for this amplifier depends too closely upon the value of β and this can heavily depend upon the temperature of the device. This is not good as devices tend to heat up during operation.

Example

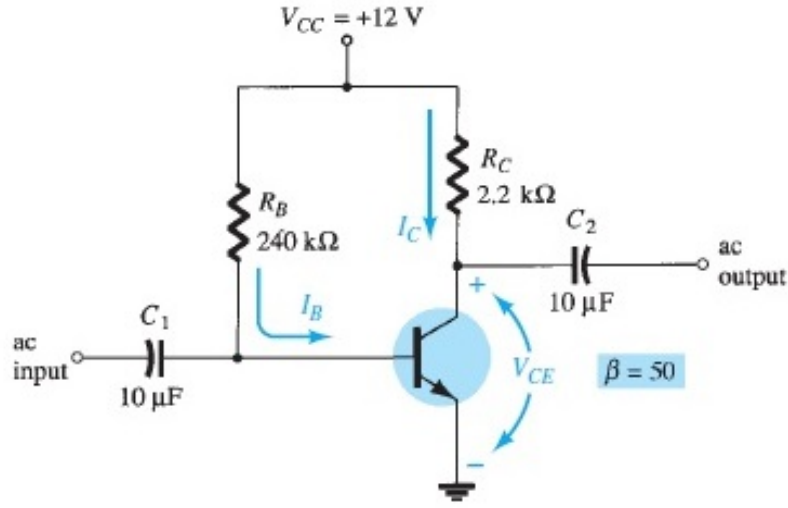
Determine the following parameters using the fixed-bias amplifier below:

- I_{BQ} and I_{CQ} .
- V_{CEQ} .
- V_B and V_C .
- V_{BC} .

Solution

$$\text{a. } I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega} = 47.08 \mu\text{A}$$

$$I_{CQ} = \beta I_{BQ} = (50)(47.08 \mu\text{A}) = 2.35 \text{ mA}$$



b. $V_{CEQ} = V_{CC} - I_C R_C$
 $= 12 \text{ V} - (2.35 \text{ mA})(2.2 \text{ k}\Omega)$
 $= 6.83 \text{ V}$

c. $V_B = V_{BE} = 0.7 \text{ V}$
 $V_C = V_{CE} = 6.83 \text{ V}$

d. Using double-subscript notation yields

$$V_{BC} = V_B - V_C = 0.7 \text{ V} - 6.83 \text{ V}$$

$$= -6.13 \text{ V}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Load line Analysis

For any values of V_{CE} and I_C , Equation (2.5) is

$$V_{CE} = V_{CC} - I_C R_C$$

$$\Rightarrow I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \quad (2.8)$$

Eqn. (2.8) is an equation of a straight line with gradient $-1/R_C$ and vertical intercept V_{CC}/R_C . The horizontal axis intercept is obtained by inserting $I_C = 0$ in Eqn. (2.8) to get $V_{CE} = V_{CC}$. This line is plotted in Fig. 2.3 and is called the DC load line. The Q-point lies on the DC load line and is given by the coordinates (V_{CEQ}, I_{CQ}) . Suppose that the signal at the base is $\pm i_B$. This signal results in a signal $i_C = \pm \beta i_B$ at the collector. The signal is always superimposed on the dc Q-point values already calculated using equations in Section (2.1.1). This affects the Q-point. For this signal, the value of I_{CQ} changes as

$$I_{CQ} \rightarrow I_{CQ} \pm \beta i_B \quad (2.9)$$

Similarly, V_{CEQ} is affected:

$$V_{CEQ} \rightarrow V_{CC} - (I_{CQ} \pm \beta i_B) R_C \quad (2.10)$$

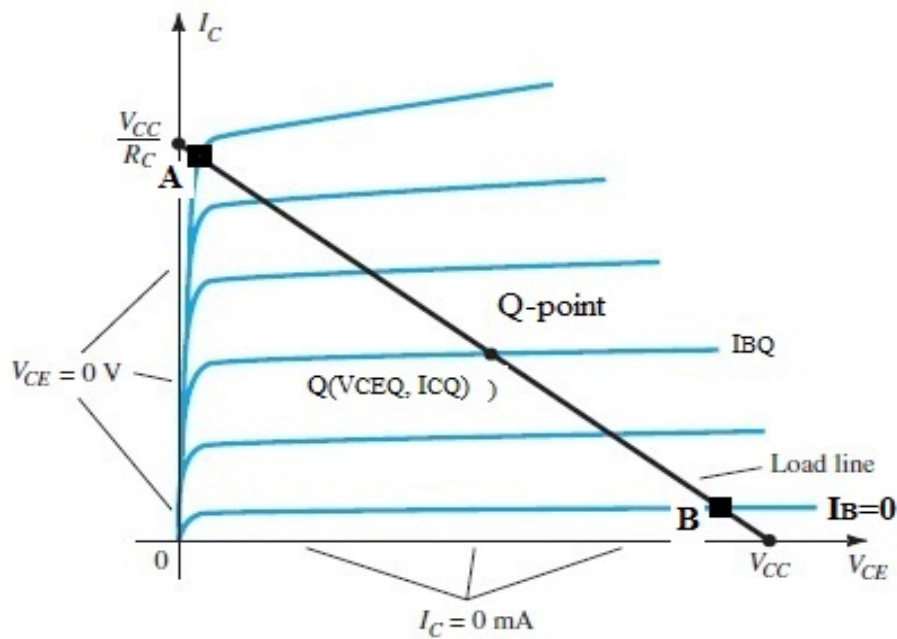
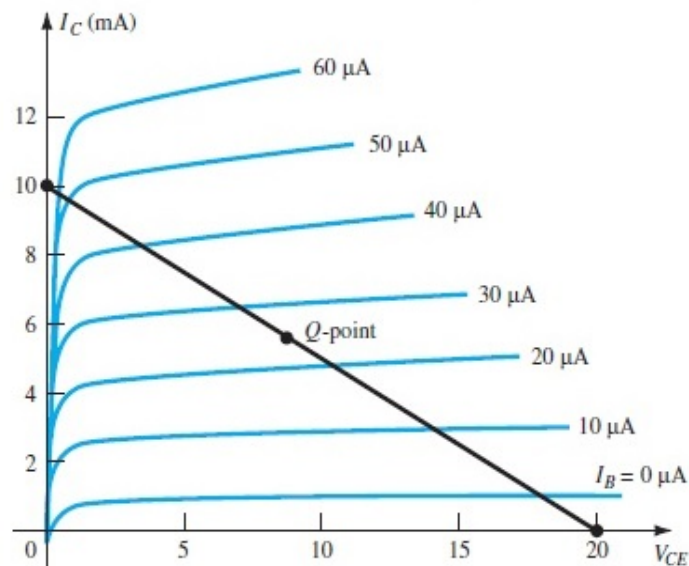


Figure 2.3: Showing the DC Load-line

Equations (2.9) and (2.10) indicate that the Q-point moves up (towards point A in Fig. 2.3) and down (towards point B) along the dc load line if a signal is fed into the amplifier. The amplifier designer must make sure that this movement of the Q-point does not drive the point up beyond point A (into saturation) or below point B (cutoff).

Example

Given the load line below and the defined Q-point, determine the required values of V_{CC} , R_C , and R_B for a fixed-bias configuration.



Solution:

$$V_{CE} = V_{CC} = 20 \text{ V at } I_C = 0 \text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{10 \text{ mA}} = 2 \text{ k}\Omega$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{25 \mu\text{A}} = 772 \text{ k}\Omega$$

2.1.2 Emitter-bias Configuration

The dc bias network of Fig. 2.4 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration seen earlier. The more stable a configuration, the less its response will change due to undesirable changes in temperature and parameter values. Fig. 2.5(a) shows the DC equivalent circuit for the emitter-bias amplifier of Fig. 2.4. Fig. 2.5(b) shows the base-emitter loop to be used for analysis. We apply Kirchoff's voltage law to the loop shown:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\text{but } I_E = (1 + \beta) I_B$$

$$\text{thus } V_{CC} - I_B R_B - V_{BE} - (1 + \beta) I_B R_E = 0$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_E} \quad (2.11)$$

Note that in Fig. 2.5(c) as compared to Fig. 2.5(b), this result is equivalent to replacing the

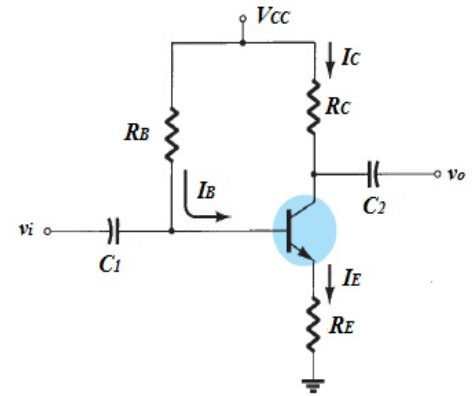


Figure 2.4:

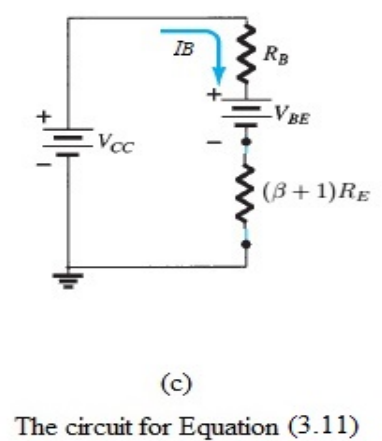
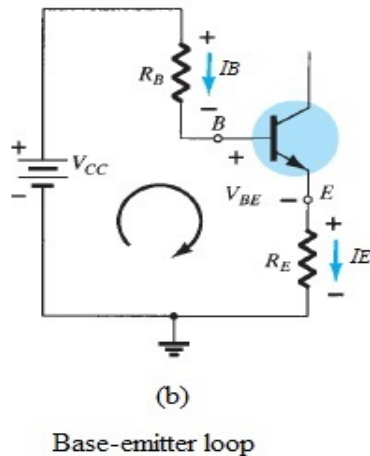
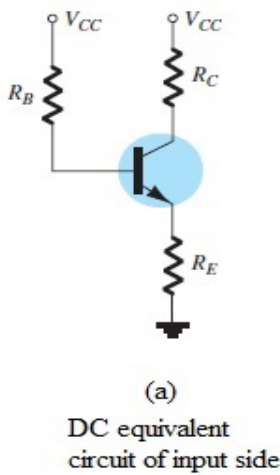


Figure 2.5: For analysing emitter-bias configured BJT.

emitter resistor R_E by $(1 + \beta)R_E$.

The output side of the amplifier may be redrawn in the form shown in Fig. 2.6. Again applying Kirchoff's voltage law to the loop shown gives

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \quad (2.12)$$

The collector current I_C is given by

$$\boxed{I_C = \beta I_B} \quad (2.13)$$

Equations (2.11), (2.12) and (2.13) specify the operating or Q-point of the emitter-bias amplifier - we can put them all together using the subscript Q as before:

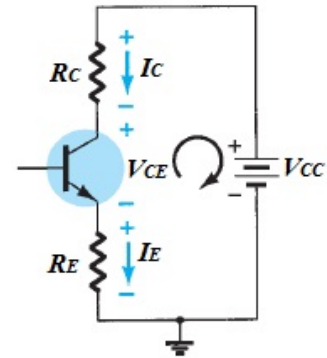


Figure 2.6: **Output**

$$\boxed{I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta)R_E}} \quad (2.14a)$$

$$I_{CQ} = \beta I_{BQ} \quad (2.14b)$$

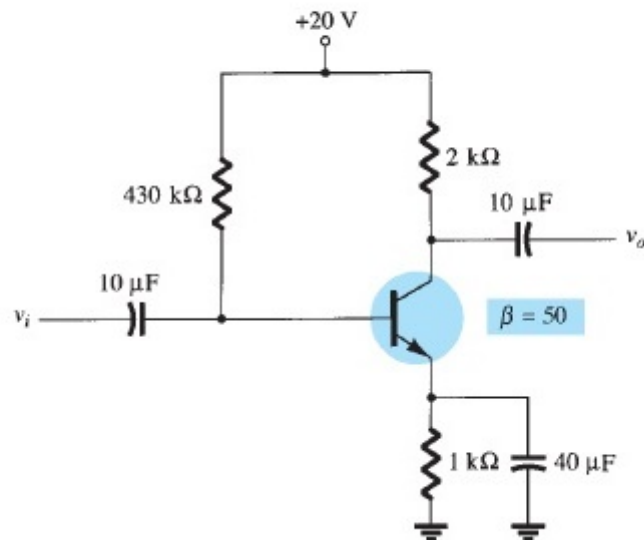
$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E) \quad (2.14c)$$

Example

Example

For the emitter-bias network below, determine:

- I_B .
- I_C .
- V_{CE} .
- V_C .
- V_E .
- V_B .
- V_{BC} .



Solution

$$\begin{aligned} \text{a. Eq. 2.11} \quad I_B &= \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{430 \text{ k}\Omega + (51)(1 \text{ k}\Omega)} \\ &= \frac{19.3 \text{ V}}{481 \text{ k}\Omega} = \mathbf{40.1 \mu A} \end{aligned}$$

$$\begin{aligned} \text{b. } I_C &= \beta I_B \\ &= (50)(40.1 \mu A) \\ &\cong \mathbf{2.01 \text{ mA}} \end{aligned}$$

$$\begin{aligned} \text{c. Eq. 2.12 : } V_{CE} &= V_{CC} - I_C(R_C + R_E) \\ &= 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega + 1 \text{ k}\Omega) = 20 \text{ V} - 6.03 \text{ V} \\ &= \mathbf{13.97 \text{ V}} \end{aligned}$$

$$\begin{aligned} \text{d. } V_C &= V_{CC} - I_C R_C \\ &= 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega) = 20 \text{ V} - 4.02 \text{ V} \\ &= \mathbf{15.98 \text{ V}} \end{aligned}$$

$$\begin{aligned} \text{e. } V_E &= V_C - V_{CE} \\ &= 15.98 \text{ V} - 13.97 \text{ V} \\ &= \mathbf{2.01 \text{ V}} \end{aligned}$$

$$\begin{aligned} \text{or } V_E &= I_E R_E \cong I_C R_E \\ &= (2.01 \text{ mA})(1 \text{ k}\Omega) \\ &= \mathbf{2.01 \text{ V}} \end{aligned}$$

$$\begin{aligned} \text{f. } V_B &= V_{BE} + V_E \\ &= 0.7 \text{ V} + 2.01 \text{ V} \\ &= \mathbf{2.71 \text{ V}} \end{aligned}$$

$$\begin{aligned} \text{g. } V_{BC} &= V_B - V_C \\ &= 2.71 \text{ V} - 15.98 \text{ V} \\ &= \mathbf{-13.27 \text{ V (reverse-biased as required)}} \end{aligned}$$

Saturation and Load line Analysis

Transistor saturation occurs if $V_{CE} \simeq 0$. If this condition is inserted into Equation (2.12), we have

$$V_{CE} = V_{CC} - I_C(R_C + R_E) = 0 \quad (2.15)$$

$$\Rightarrow I_C = \frac{V_{CC}}{R_C + R_E} \quad (2.16)$$

$$\text{The saturation current is } I_{CSAT} = I_C \Big|_{V_{CE}=0} = \frac{V_{CC}}{R_C + R_E} \quad (2.17)$$

The effect on the DC load line of including an emitter resistance R_E is shown in Fig. 2.7 - basically the load I_{CSAT} is lowered since

$$\text{without } R_E, \quad I_{CSAT} = \frac{V_{CC}}{R_C} > \frac{V_{CC}}{R_C + R_E} \quad \text{with } R_E$$

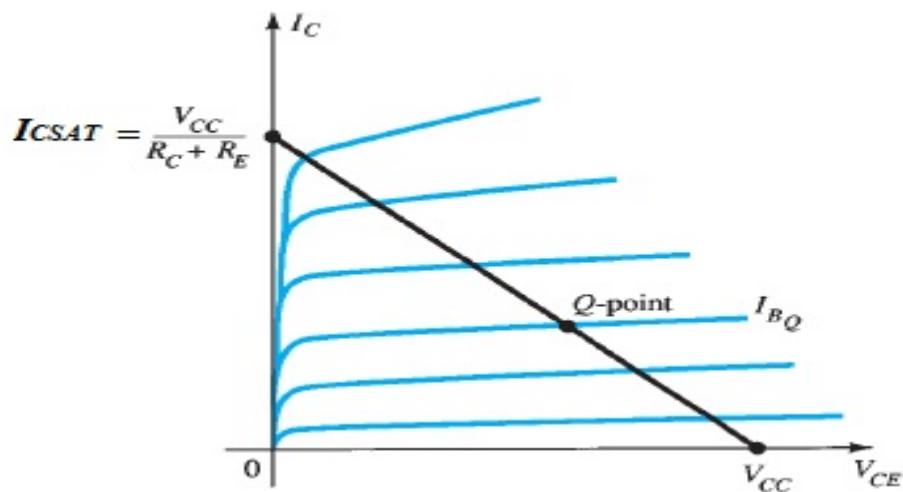


Figure 2.7: DC load-line for emitter-bias configuration

Example

Example

- Draw the load line for the network of Fig. 2.8(a) on the characteristics for the transistor appearing in Fig. 2.8(b)
- For a Q -point at the intersection of the load line with a base current of $15\ \mu\text{A}$, find the values of I_{CQ} and V_{CEQ} .
- Determine the dc beta at the Q -point.
- Using the beta for the network determined in part c, calculate the required value of R_B and suggest a possible standard value.

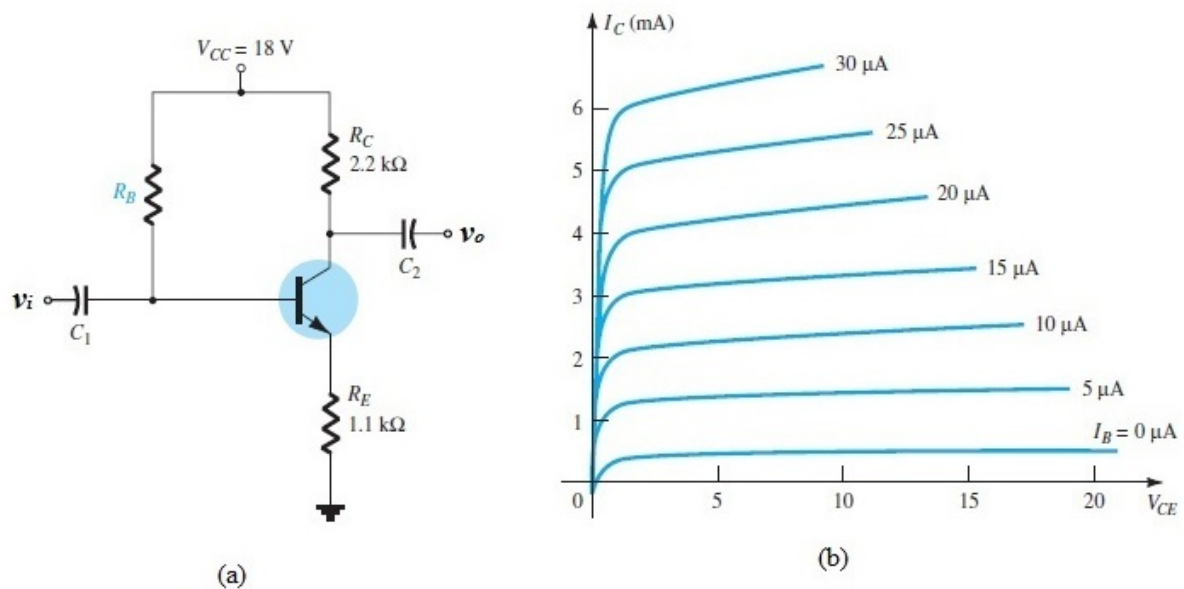


Figure 2.8:

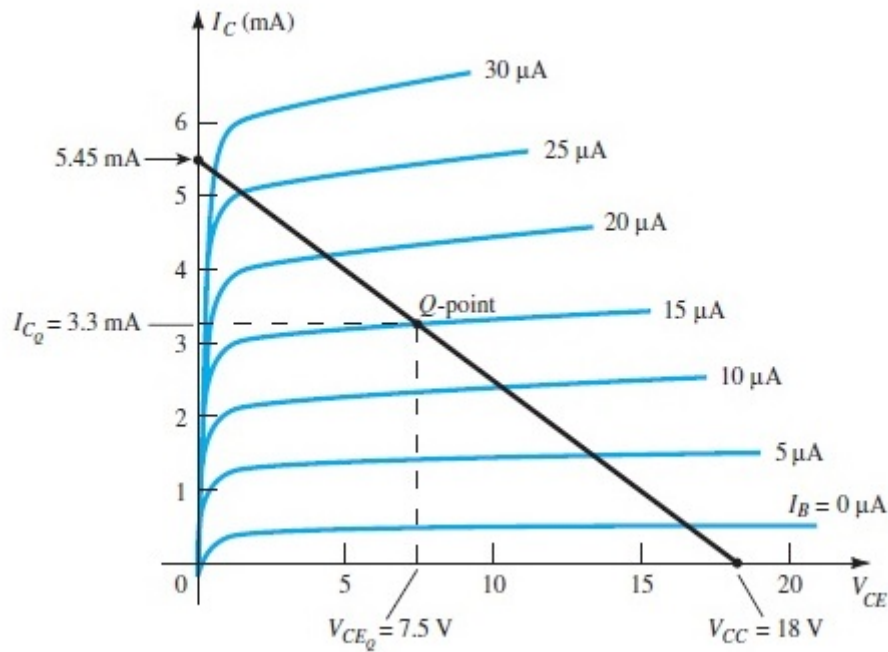


Figure 2.9:

Solution

- a. Two points on the characteristics are required to draw the load line.

$$\text{At } V_{CE} = 0 \text{ V: } I_C = \frac{V_{CC}}{R_C + R_E} = \frac{18 \text{ V}}{2.2 \text{ k}\Omega + 1.1 \text{ k}\Omega} = \frac{18 \text{ V}}{3.3 \text{ k}\Omega} = 5.45 \text{ mA}$$

$$\text{At } I_C = 0 \text{ mA: } V_{CE} = V_{CC} = 18 \text{ V}$$

The resulting load line appears in Fig. 2.9 .

- b. From the characteristics of Fig. 2.9 we find

$$V_{CE_Q} \cong 7.5 \text{ V}, I_{C_Q} \cong 3.3 \text{ mA}$$

- c. The resulting dc beta is:

$$\beta = \frac{I_{C_Q}}{I_{B_Q}} = \frac{3.3 \text{ mA}}{15 \mu\text{A}} = 220$$

- d. Applying Eq. 2.11:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{18 \text{ V} - 0.7 \text{ V}}{R_B + (220 + 1)(1.1 \text{ k}\Omega)}$$

$$\text{and } 15 \mu\text{A} = \frac{17.3 \text{ V}}{R_B + (221)(1.1 \text{ k}\Omega)} = \frac{17.3 \text{ V}}{R_B + 243.1 \text{ k}\Omega}$$

$$\text{so that } (15 \mu\text{A})(R_B) + (15 \mu\text{A})(243.1 \text{ k}\Omega) = 17.3 \text{ V}$$

$$\text{and } (15 \mu\text{A})(R_B) = 17.3 \text{ V} - 3.65 \text{ V} = 13.65 \text{ V}$$

$$\text{resulting in } R_B + \frac{13.65 \text{ V}}{15 \mu\text{A}} = 910 \text{ k}\Omega$$

2.1.3 Voltage-Divider Bias Configuration

In the previous bias configurations the bias collector current I_{CQ} and voltage V_{CEQ} were a function of the forward current gain β of the transistor. However, because β is temperature sensitive, especially for silicon transistors, and the actual value of β is usually not precisely known, it would be desirable to develop a bias circuit that is less dependent on, or in fact is independent of, the transistor's β . The voltage-divider bias configuration of Fig. 2.10(a) is such a network. Fig. 2.10(b) shows the Q point and DC load-line on the output characteristics. The DC equivalent

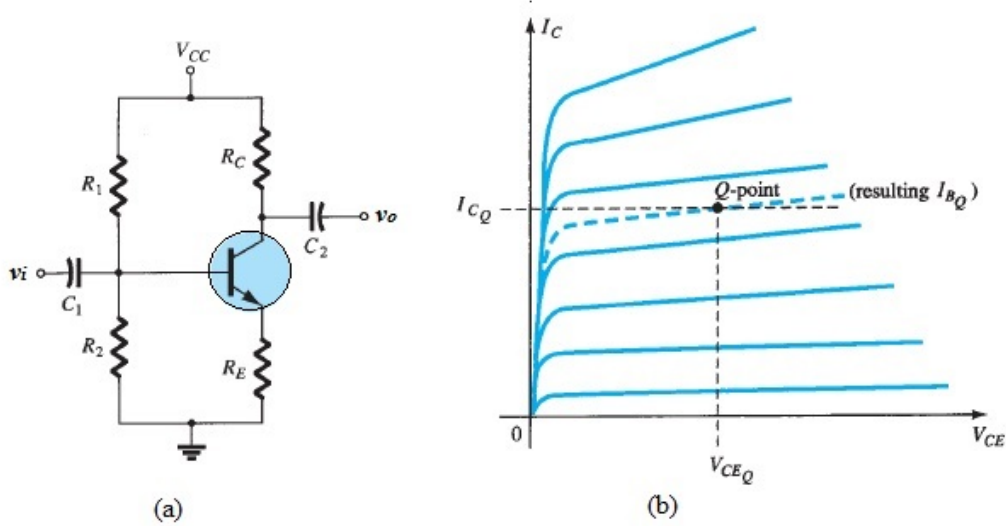


Figure 2.10: (a) Voltage-divide bias network (b) output characteristics

circuit for the voltage-divider bias circuit of Fig. 2.10(a) is shown in Fig. 2.11(a). We apply

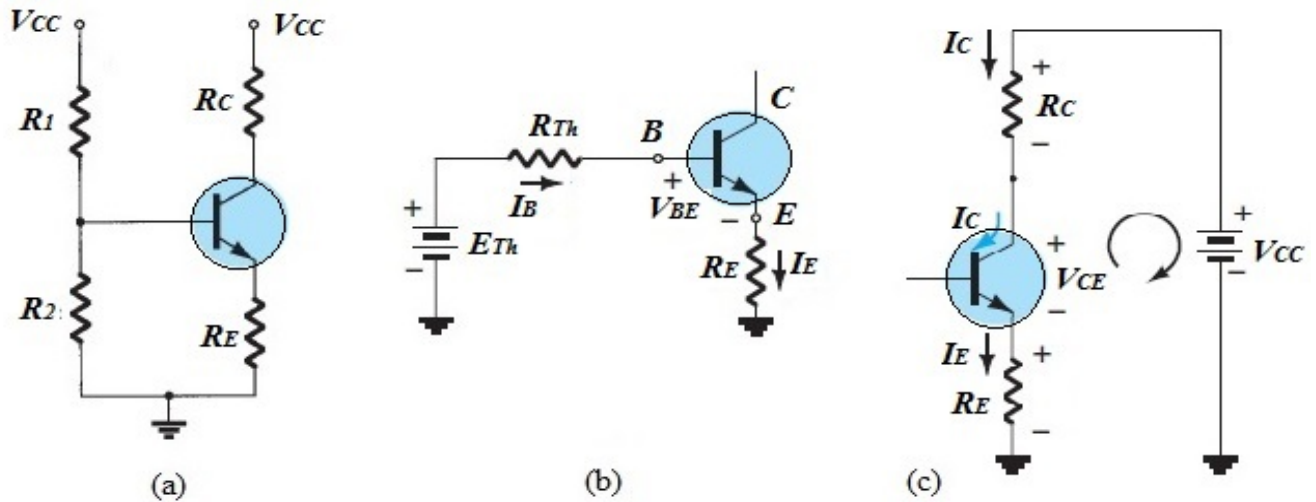


Figure 2.11: Voltage-divider (a) circuit (b) Thevenin equivalent circuit of input (c) circuit of output

Thevenin's theorem to reduce the circuit to a series combination of source E_{Th} and equivalent

resistance R_{Th} as in Fig. 2.11(b) where

$$R_{Th} = R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2} \quad (2.18a)$$

$$E_{Th} = \frac{R_2}{R_1 + R_2} V_{CC} \quad (2.18b)$$

The base current I_B may be calculated using Fig. 2.11(b) as follows:

$$\begin{aligned} E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E &= 0 \\ \text{but } I_E &= (1 + \beta) I_B \\ \Rightarrow E_{Th} - I_B R_{Th} - V_{BE} - (1 + \beta) I_B R_E &= 0 \end{aligned}$$

so that

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (1 + \beta) R_E} \quad (2.19)$$

The output side of the amplifier may be analysed using Fig. 2.11(c). We apply Kirchoff's voltage law to the loop:

$$\begin{aligned} V_{CC} - I_C R_C - V_{CE} - I_E R_E &= 0 \\ \text{but } I_E &= \frac{1 + \beta}{\beta} I_C \\ \Rightarrow V_{CC} - I_C R_C - V_{CE} - \frac{1 + \beta}{\beta} I_C R_E &= 0 \end{aligned}$$

The collector-emitter voltage V_{CE} is then given by

$$V_{CE} = V_{CC} - I_C \left[R_C + \left(\frac{1 + \beta}{\beta} \right) R_E \right] \quad (2.20)$$

Provided that $\beta \gg 1$, which is normally the case, Equation 2.20 may be written as

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \quad (2.21)$$

Eqn. (2.21) is exactly the same as that obtained for V_{CE} (Eqn. (2.12)) for the emitter-bias configuration. This is expected as the output circuit for both is exactly the same. The Q-point parameters for the voltage-divider configuration are summarised, using the Q subscript as

$$I_{BQ} = \frac{E_{Th} - V_{BE}}{R_{Th} + (1 + \beta) R_E} \quad (2.22a)$$

$$I_{CQ} = \beta I_{BQ} \quad (2.22b)$$

$$V_{CEQ} = V_{CC} - I_{CQ} (R_C + R_E) \quad (2.22c)$$

Example

Example

Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of the figure below:

Solution

$$\begin{aligned} \text{Equation (18a): } R_{Th} &= R_1 \parallel R_2 \\ &= \frac{(39 \text{ k}\Omega)(3.9 \text{ k}\Omega)}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 3.55 \text{ k}\Omega \end{aligned}$$

$$\begin{aligned} \text{Equation (18b): } E_{Th} &= \frac{R_2 V_{CC}}{R_1 + R_2} \\ &= \frac{(3.9 \text{ k}\Omega)(22 \text{ V})}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 2 \text{ V} \end{aligned}$$

$$\begin{aligned} \text{Equation (19): } I_B &= \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \\ &= \frac{2 \text{ V} - 0.7 \text{ V}}{3.55 \text{ k}\Omega + (101)(1.5 \text{ k}\Omega)} = \frac{1.3 \text{ V}}{3.55 \text{ k}\Omega + 151.5 \text{ k}\Omega} \\ &= 8.38 \mu\text{A} \\ I_C &= \beta I_B \quad \text{e.g from Equation (2.21b)} \\ &= (100)(8.38 \mu\text{A}) \\ &= 0.84 \text{ mA} \end{aligned}$$

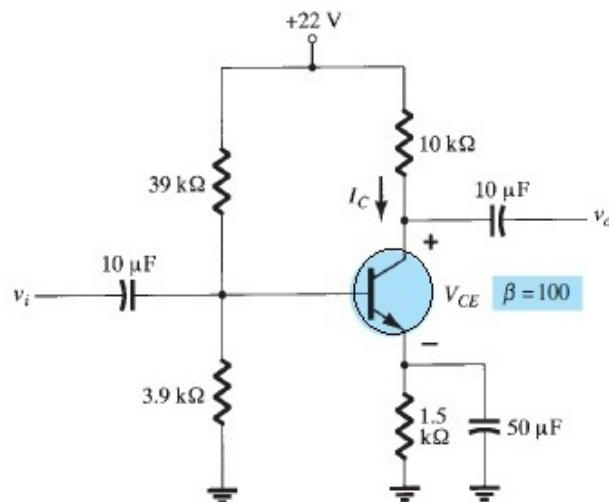


FIG. 4.35

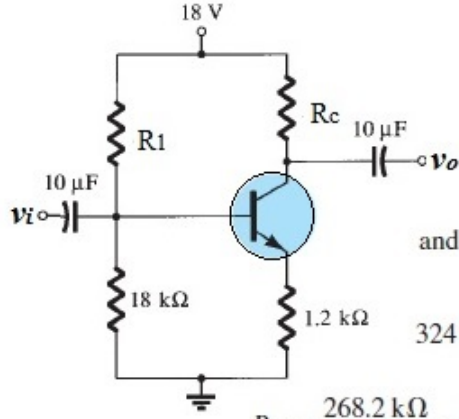
Beta-stabilized circuit for Example 4.8.

$$\begin{aligned} \text{Equation (2.20): } V_{CE} &= V_{CC} - I_C(R_C + R_E) \\ &= 22 \text{ V} - (0.84 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega) \\ &= 22 \text{ V} - 9.66 \text{ V} \\ &= 12.34 \text{ V} \end{aligned}$$

Example:

Given that $I_{CQ} = 2 \text{ mA}$ and $V_{CEQ} = 10 \text{ V}$, determine R_1 and R_C for the circuit below:

Solution:



$$V_E = I_E R_E \cong I_C R_E = (2 \text{ mA})(1.2 \text{ k}\Omega) = 2.4 \text{ V}$$

$$V_B = V_{BE} + V_E = 0.7 \text{ V} + 2.4 \text{ V} = 3.1 \text{ V}$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1 \text{ V}$$

$$\text{and } \frac{(18 \text{ k}\Omega)(18 \text{ V})}{R_1 + 18 \text{ k}\Omega} = 3.1 \text{ V}$$

$$324 \text{ k}\Omega = 3.1 R_1 + 55.8 \text{ k}\Omega$$

$$R_1 = \frac{268.2 \text{ k}\Omega}{3.1} = 86.52 \text{ k}\Omega \quad R_C = \frac{V_{RC}}{I_C} = \frac{V_{CC} - V_C}{I_C}$$

$$\text{with } V_C = V_{CE} + V_E = 10 \text{ V} + 2.4 \text{ V} = 12.4 \text{ V}$$

$$\text{and } R_C = \frac{18 \text{ V} - 12.4 \text{ V}}{2 \text{ mA}} = 2.8 \text{ k}\Omega$$

Approximate Biasing for Voltage-Divider

We consider Fig. 2.10(a) again. The potential at the base is assumed to be

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} \quad (2.23)$$

since R_1 and R_2 are assumed to be in series. The voltage-divider may be redrawn as shown in Fig. 2.12 where R_i is the input impedance of the rest of the amplifier (everything to the right of the base, B). R_1 and R_2 are therefore not in series. Some current must flow through R_i .

A base current I_B flows into the rest of amplifier through a resistance R_i . The current I_B depends upon R_i and ideally, this current must be very small in order that the potential at B remains fixed i.e. R_1 and R_2 appear to be in series. So $I_B \ll I_1$ and I_2 or $I_1 \cong I_2$. This will only be the case if R_i is much larger than either of R_1 and R_2 . Because $R_i = (1 + \beta)R_E \cong \beta R_E$, the condition for the potential-divider assumption is

$$\beta R_E \geq 10 R_2 \quad (2.24)$$

As we have seen earlier, the emitter and collector currents are related by $I_E = (1 + \beta)I_C$ but as we also know, values of β range from 50 to 300, so the assumption $\beta \gg 1$ is justified. In this case, we can use the approximation

$$I_E \cong I_C \quad (2.25)$$

in all biasing designs.

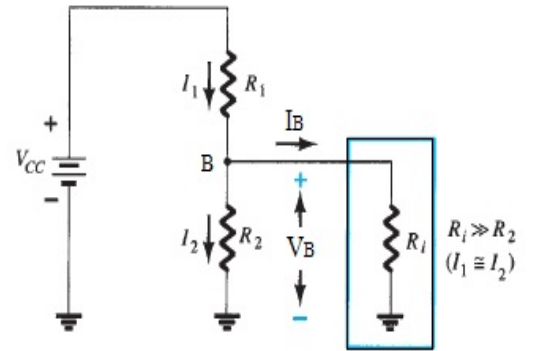


Figure 2.12:

Example

Determine the levels of I_{CQ} and V_{CEQ} for the voltage-divider configuration of Fig. 4.37 using the exact and approximate techniques and compare solutions. In this case, the conditions of Eq. (2.23) *will not be satisfied* and the results will reveal the difference in solution if the criterion of Eq. (2.23) is ignored.

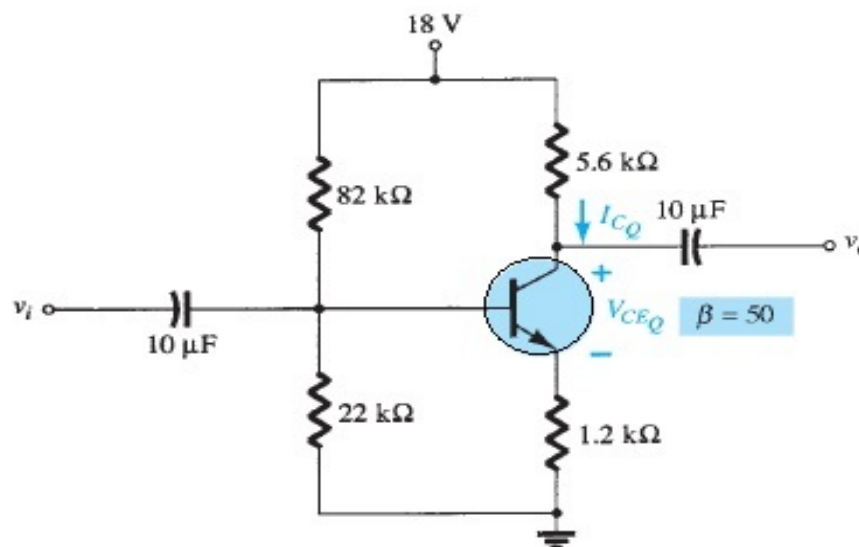


FIG. 4.37

Solution:

Exact analysis:

Eq. (2.23):

$$\beta R_E \geq 10 R_2$$

$$(50)(1.2 \text{ k}\Omega) \geq 10(22 \text{ k}\Omega)$$

$$60 \text{ k}\Omega \not\geq 220 \text{ k}\Omega \text{ (not satisfied)}$$

$$R_{Th} = R_1 \parallel R_2 = 82 \text{ k}\Omega \parallel 22 \text{ k}\Omega = 17.35 \text{ k}\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22 \text{ k}\Omega (18 \text{ V})}{82 \text{ k}\Omega + 22 \text{ k}\Omega} = 3.81 \text{ V}$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{3.81 \text{ V} - 0.7 \text{ V}}{17.35 \text{ k}\Omega + (51)(1.2 \text{ k}\Omega)} = \frac{3.11 \text{ V}}{78.55 \text{ k}\Omega} = 39.6 \mu\text{A}$$

$$I_{CQ} = \beta I_B = (50)(39.6 \mu\text{A}) = 1.98 \text{ mA}$$

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\ &= 18 \text{ V} - (1.98 \text{ mA})(5.6 \text{ k}\Omega + 1.2 \text{ k}\Omega) \\ &= 4.54 \text{ V} \end{aligned}$$

Approximate analysis:

$$\begin{aligned}
 V_B &= E_{Th} = 3.81 \text{ V} \\
 V_E &= V_B - V_{BE} = 3.81 \text{ V} - 0.7 \text{ V} = 3.11 \text{ V} \\
 I_{CQ} &\cong I_E = \frac{V_E}{R_E} = \frac{3.11 \text{ V}}{1.2 \text{ k}\Omega} = 2.59 \text{ mA} \\
 V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\
 &= 18 \text{ V} - (2.59 \text{ mA})(5.6 \text{ k}\Omega + 1.2 \text{ k}\Omega) \\
 &= 3.88 \text{ V}
 \end{aligned}$$

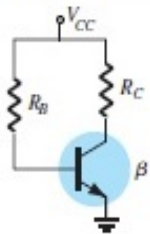
Tabulating the results, we have:

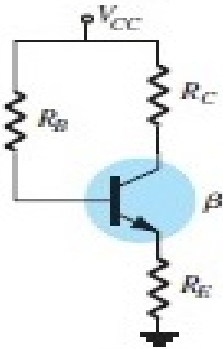
Comparing the exact and approximate approaches.

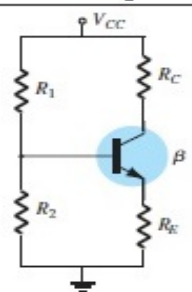
	$I_{CQ} \text{ (mA)}$	$V_{CEQ} \text{ (V)}$
Exact	1.98	4.54
Approximate	2.59	3.88

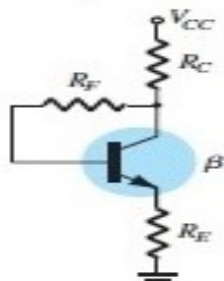
The results reveal the difference between exact and approximate solutions. I_{CQ} is about 30% greater with the approximate solution, whereas V_{CEQ} is about 10% less. The results are notably different in magnitude, but even though βR_E is only about three times larger than R_2 , the results are still relatively close to each other. For the future, however, our analysis will be dictated by Eq. (2.23) to ensure a close similarity between exact and approximate solutions.

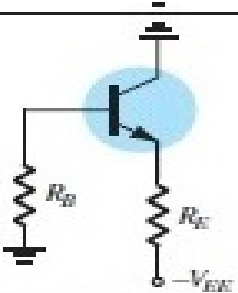
Table: BJT Bias Configurations

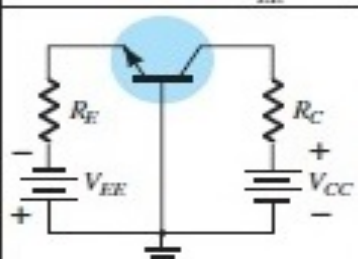
Type	Configuration	Pertinent Equations
Fixed-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C R_C$

Emitter-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $R_i = (\beta + 1)R_E$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$
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Voltage-divider bias		EXACT: $R_{Th} = R_1 \parallel R_2$, $E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$ APPROXIMATE: $\beta R_E \geq 10 R_2$ $I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$ $I_C = \beta I_B$, $I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$ $V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$, $V_E = V_B - V_{BE}$ $I_E = \frac{V_E}{R_E}$, $I_B = \frac{I_E}{\beta + 1}$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
----------------------	--	---

Collector-feedback		$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$ $I_C = \beta I_B$, $I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
--------------------	---	--

Emitter-follower		$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B$, $I_E = (\beta + 1)I_B$ $V_{CE} = V_{EE} - I_E R_E$
------------------	--	---

Common-base		$I_E = \frac{V_{EE} - V_{BE}}{R_E}$ $I_B = \frac{I_E}{\beta + 1}$, $I_C = \beta I_B$ $V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$ $V_{CB} = V_{CC} - I_C R_C$
-------------	---	---

2.2 Emitter-follower Configuration

Fig. 2.13(a) shows yet another manner in which a BJT can be configured, called the emitter-follower or common-collector configuration. Note that the collector terminal is common to both input v_i and output v_o . Fig. 2.13(b) is the DC equivalent circuit of the circuit of Fig. 2.13(a) which we shall now use for analysis. Applying Kirchoff's voltage law to the inout side, we have

$$\begin{aligned}
 -I_B R_b - V_{BE} - I_E R_E + V_{EE} &= 0 \\
 \text{but } I_E &= (1 + \beta)I_B \\
 \text{so that } -I_B R_B - V_{BE} - (1 + \beta)I_B R_E + V_{EE} &= 0
 \end{aligned}$$

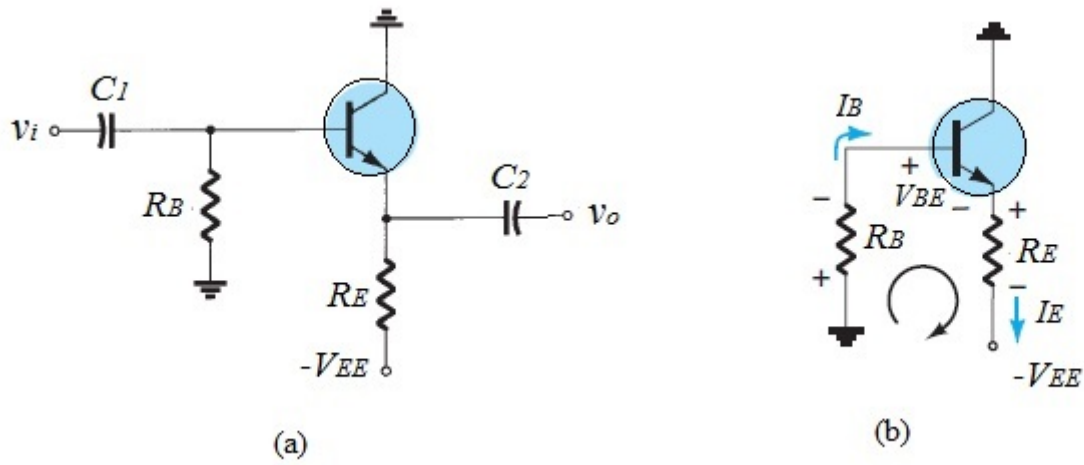


Figure 2.13:

$$\Rightarrow I_B = \frac{V_{EE} - V_{BE}}{R_B + (1 + \beta)R_E} \quad (2.26)$$

On the output side,

$$-V_{EE} - I_E R_E + V_{EE} = 0 \quad (2.27)$$

$$\Rightarrow V_{CE} = V_{EE} - I_E R_E \quad (2.28)$$

As before,

$$\Rightarrow I_C = \beta I_B \quad (2.29)$$

The three equations 2.26, 2.28 and 2.29 are the basic biasing equations for the emitter-follower, and specify the Q-point for the configurations:

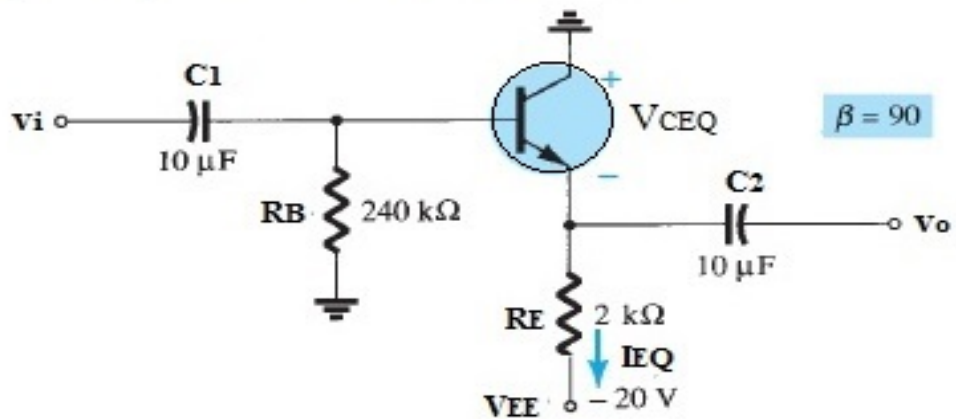
$$I_{BQ} = \frac{V_{EE} - V_{BE}}{R_B + (1 + \beta)R_E} \quad (2.30a)$$

$$I_{CQ} = \beta I_{BQ} \quad (2.30b)$$

$$V_{CEQ} = V_{EE} - (\beta + 1)I_{BQ}R_E \quad (2.30c)$$

Example:

Determine V_{CEQ} and I_{EQ} for the network of circuit below:

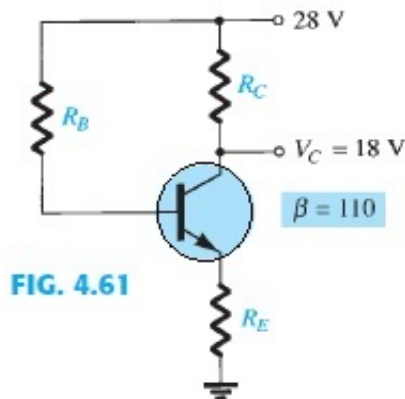


Solution:

$$\begin{aligned}
 \text{Eq. 2.26/2.30a: } I_B &= \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E} \\
 &= \frac{20 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega + (90 + 1)2 \text{ k}\Omega} = \frac{19.3 \text{ V}}{240 \text{ k}\Omega + 182 \text{ k}\Omega} \\
 &= \frac{19.3 \text{ V}}{422 \text{ k}\Omega} = 45.73 \mu\text{A}
 \end{aligned}$$

$$\begin{aligned}
 \text{and Eq. 2.28/2.30c: } V_{CE_Q} &= V_{EE} - I_E R_E \\
 &= V_{EE} - (\beta + 1)I_B R_E \\
 &= 20 \text{ V} - (90 + 1)(45.73 \mu\text{A})(2 \text{ k}\Omega) \\
 &= 20 \text{ V} - 8.32 \text{ V} \\
 &= 11.68 \text{ V}
 \end{aligned}$$

Example : The emitter-bias configuration of Fig. 4.61 has the following specifications: $I_{C_Q} = \frac{1}{2}I_{C_{\text{sat}}}$, $I_{C_{\text{sat}}} = 8 \text{ mA}$, $V_C = 18 \text{ V}$, and $\beta = 110$. Determine R_C , R_E , and R_B .



$$\begin{aligned}
 \text{Solution: } I_{C_Q} &= \frac{1}{2}I_{C_{\text{sat}}} = 4 \text{ mA} \\
 R_C &= \frac{V_{R_C}}{I_{C_Q}} = \frac{V_{CC} - V_C}{I_{C_Q}} \\
 &= \frac{28 \text{ V} - 18 \text{ V}}{4 \text{ mA}} = 2.5 \text{ k}\Omega \\
 I_{C_{\text{sat}}} &= \frac{V_{CC}}{R_C + R_E} \\
 \text{and } R_C + R_E &= \frac{V_{CC}}{I_{C_{\text{sat}}}} = \frac{28 \text{ V}}{8 \text{ mA}} = 3.5 \text{ k}\Omega \\
 R_E &= 3.5 \text{ k}\Omega - R_C \\
 &= 3.5 \text{ k}\Omega - 2.5 \text{ k}\Omega \\
 R_E &= 1 \text{ k}\Omega
 \end{aligned}$$

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{4 \text{ mA}}{110} = 36.36 \mu\text{A}$$

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$\text{and } R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{BQ}}$$

$$\begin{aligned} \text{with } R_B &= \frac{V_{CC} - V_{BE}}{I_{BQ}} - (\beta + 1)R_E \\ &= \frac{28 \text{ V} - 0.7 \text{ V}}{36.36 \mu\text{A}} - (111)(1 \text{ k}\Omega) \\ &= \frac{27.3 \text{ V}}{36.36 \mu\text{A}} - 111 \text{ k}\Omega \\ &= 639.8 \text{ k}\Omega \end{aligned}$$

For standard values,

$R_C = 2.4 \text{ k}\Omega$	$R_E = 1 \text{ k}\Omega$	$R_B = 620 \text{ k}\Omega$
-----------------------------	---------------------------	-----------------------------

Example:

Consider first the design of the dc bias components of an amplifier circuit having emitter-resistor bias stabilization as shown in Fig. 4.62. The supply voltage and operating point were selected from the manufacturer's information on the transistor used in the amplifier.

The selection of collector and emitter resistors cannot proceed directly from the information just specified. The equation that relates the voltages around the collector-emitter loop has two unknown quantities present—the resistors R_C and R_E . At this point some engineering judgment must be made, such as the level of the emitter voltage compared to the applied supply voltage. Recall that the need for including a resistor from emitter to ground was to provide a means of dc bias stabilization so that the change of collector current due to leakage currents in the transistor and the transistor beta would not cause a large shift in the operating point. The emitter resistor cannot be unreasonably large because the voltage across it limits the range of swing of the voltage from collector to emitter (to be noted when the ac response is discussed). The examples examined in this chapter reveal that the voltage from emitter to ground is typically around one-fourth to one-tenth of the supply voltage. Selecting the conservative case of one-tenth will permit calculating the emitter resistor R_E and the resistor R_C in a manner similar to the examples just completed. In the next example we perform a complete design of the network of Fig. 4.62 using the criteria just introduced for the emitter voltage.

Example:

Determine the resistor values for the circuit for the indicated operating point and supply voltage. Ignore all capacitors for this problem and use approximation.

Solution:

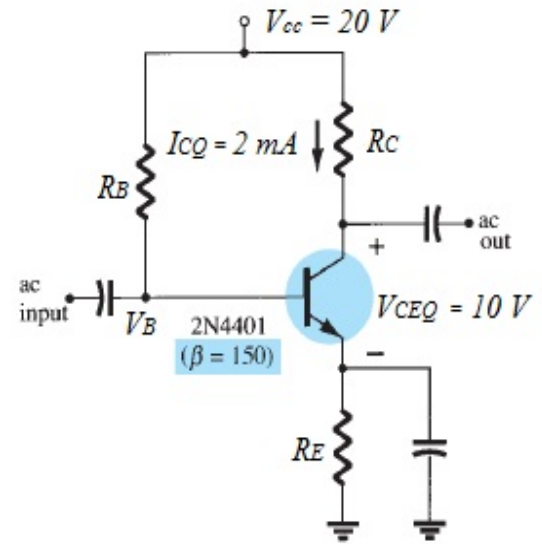
$$V_E = \frac{1}{10}V_{CC} = \frac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{2\text{ mA}} = 1\text{ k}\Omega$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 10\text{ V} - 2\text{ V}}{2\text{ mA}} = \frac{8\text{ V}}{2\text{ mA}} = 4\text{ k}\Omega$$

$$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{150} = 13.33\text{ }\mu\text{A}$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20\text{ V} - 0.7\text{ V} - 2\text{ V}}{13.33\text{ }\mu\text{A}} \cong 1.3\text{ M}\Omega$$



2.3 Multistage Amplifiers

Amplifier circuits so far considered have been single stage amplifiers. In practice, amplifiers may have many similar stages, forming what is called multistage amplifiers.

2.3.1 RC Coupled Voltage-Divider Amplifier

Fig. 2.14(a) is a two-stage RC coupled voltage-divider amplifier and Fig. 2.14(b) is its dc equivalent circuit. The term RC coupled is used to indicate that an RC network is used to couple the two stages. The first stage is a voltage-divider amplifier based around transistor Q_1 and the second stage is exactly the same but based around transistor Q_2 . The two stages are connected or coupled through an RC network formed using resistor R_C and capacitor C_C . Stage 2 ends at the second capacitor C_C . The output signal v_o is coupled to the load R_L through second capacitor C_C .

Fig. 2.14(b) is the DC equivalent circuit of Fig. 2.14(a). Note that there are no capacitors (the are open circuited) and no AC signals, such as v_s and v_o that appear in Fig. 2.14(a). The analysis of each stage follows the same method used for single stage amplifier considered in Section 2.2.

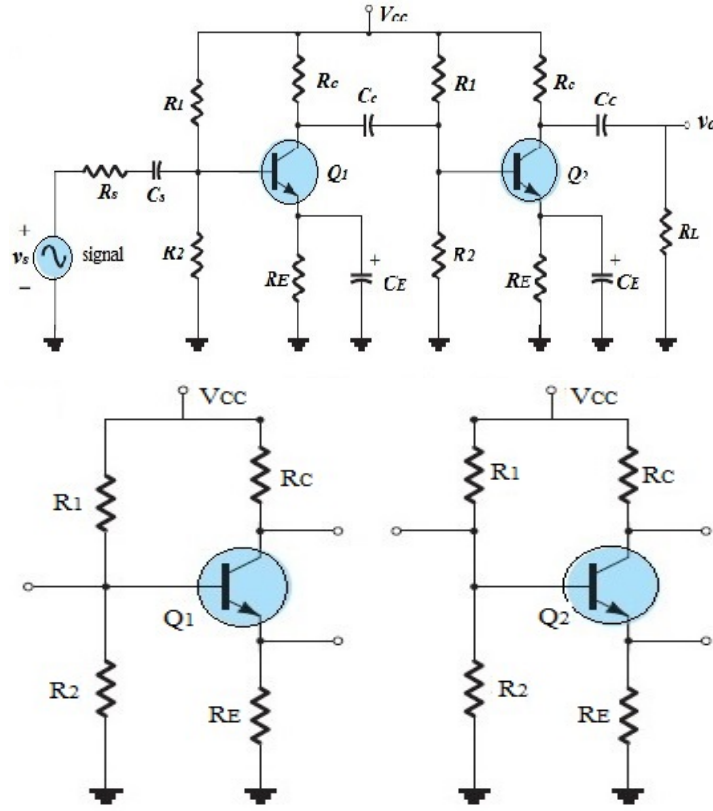


Figure 2.14: Two-stage RC coupled voltage-divider amplifier (a) circuit (b) DC equivalent

2.3.2 Darlington BJT configuration

The use of multistage amplifiers is primarily to get more gain. Instead of using such multistage amplifiers, one may use a special connection called the Darlington configuration. Fig. 2.15(a) is a base-bias amplifier using the Darlington configuration. For dc, capacitors C_s and C_C cut R_S and R_L out and we end up with the dc equivalent circuit of Fig. 2.15(b). Note that the emitter of Q_1 is connected to the base of Q_2 and the collectors of both Q_1 and Q_2 are connected together. This effectively forms one composite transistor with input current base current I_{B1} and collector current I_{C2} . We let the forward current amplification ratios for Q_1 and Q_2 be β_1 and β_2 respectively. Note that for this connection, $I_{E1} = I_{B2}$. The gain of the combined transistors is

$$\begin{aligned}\beta_D &= I_{C2}/I_{B1} \\ \text{but } I_{C2} &= \beta_2 I_{B2} = \beta_2 I_{E1} = \beta_2 (1 + \beta_1) I_{B1} \\ \Rightarrow \beta_D &= I_{C21}/I_{B1} = \beta_2(1 + \beta_1)\end{aligned}$$

If $\beta_1 \gg 1$ as is usually the case, then $(1 + \beta_1) \simeq \beta_1$ and

$$\boxed{\beta_D \simeq \beta_1 \beta_2} \quad (2.31)$$

Eqn. 2.31 gives the effective amplification of two transistors connected as a Darlington pair. For the 2N4123 featured in Chapter 1 for example, the data sheet gives $\beta = h_{fe}$ from 50 to 200. Using two such transistors connected as a Darlington pair would produce an effective β_D from a minimum of 2500 to a maximum of 40,000 - which is a phenomenal amplification! Further analysis

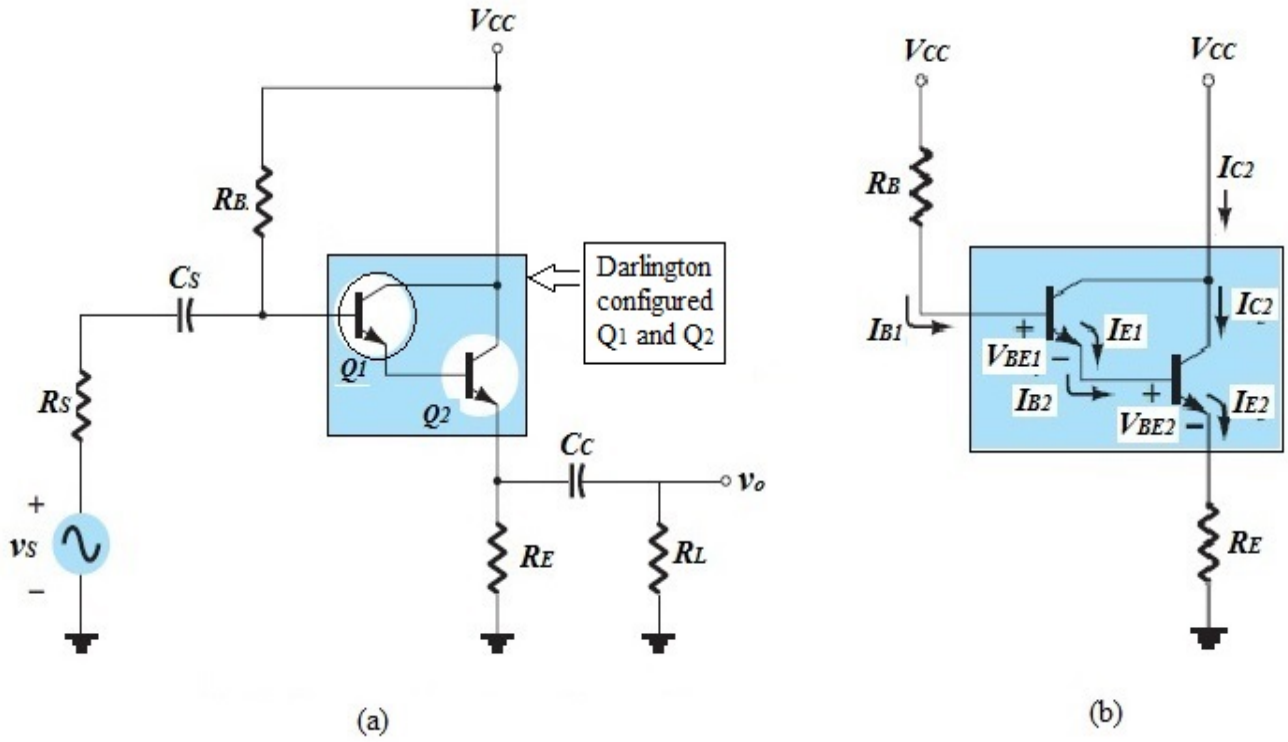


Figure 2.15: **Darlington BJT (a) amplifier (b) its DC equivalent circuit.**

shows that

$$I_{B1} = \frac{V_{CC} - V_{BE1} - V_{BE2}}{R_B + (1 + \beta_D)R_E}$$

Let $V_{BED} = V_{BE1} + V_{BE2}$

$$I_{B1} = \frac{V_{CC} - V_{BED}}{R_B + (1 + \beta_D)R_E} \quad (2.32)$$

Eqn. 2.32 is similar to that for a single stage amplifier (for example Eqn. 2.19), with the exception that β_D replaces β . For the currents

$$I_{C2} \simeq I_{E2} = \beta_D I_{B1} \quad (2.33)$$

and the dc voltage at the emitter is

$$V_{E2} = I_{E2}R_E$$

The collector voltage is equal to the supply voltage V_{CC}

$$V_{C2} = V_{CC} \quad (2.34)$$

and the voltage across the transistor output is

$$V_{CE2} = V_{C2} - V_{E2} \quad (2.35)$$

and

$$V_{CE2} = V_{CC} - V_{E2} \quad (2.36)$$

Eqns. 2.32, 2.33 and 2.36 may be taken as the Q-point values for this configuration.

$$I_{BQ} = \frac{V_{CC} - V_{BED}}{R_B + (1 + \beta_D)R_E} \quad (2.37a)$$

$$I_{CQ} = I_{C2} \simeq I_{E2} = \beta_D I_{BQ} \quad (2.37b)$$

$$V_{CEQ} = V_{CC} - V_{E2} = V_{CC} - I_{CQ}R_E \quad (2.37c)$$

since $V_{E2} = I_{E2}R_E \simeq I_{C2}R_E = \beta_D I_{BQ}R_E$ as $I_{E2} \simeq I_{C2}$. Eqns. (2.37) define the Q-point for the amplifier of Fig.2.15.

2.3.3 The Cascode Configured Amplifier

Another important multistage transistor configuration for amplifier design is the Cascode configuration. Again this uses two transistors. Fig. 2.16(a) is one such design, showing the biasing aspects. Note that the emitter of transistor Q_1 feeds into the collector of transistor Q_2 . The input is at the base of Q_2 through capacitor C_s . Fig. 2.16(b) is the dc equivalent circuit for analysis. A basic assumption of the analysis of this circuit is that the current that flows down from V_{CC}

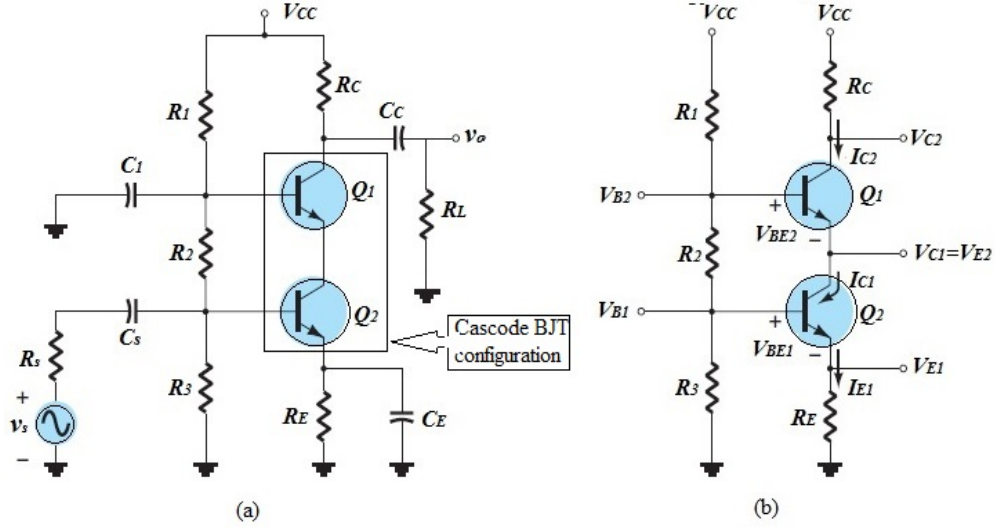


Figure 2.16: **Cascode configuration: (a) circuit (b) dc equivalent circuit**

through resistors R_1 , R_2 and R_3 is much larger than that which flows into the bases of Q_1 and Q_2 . R_1 , R_2 and R_3 therefore form a 3-section voltage divider. $R_2 + R_3$ set the potential at the base of Q_1 at

$$V_{B1} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} V_{CC} \quad (2.38)$$

and R_3 sets the voltage at the base of Q_2 at

$$V_{B2} = \frac{R_3}{R_1 + R_2 + R_3} V_{CC} \quad (2.39)$$

The emitter potentials are

$$V_{E1} = V_{B1} - V_{BE1} \quad (2.40a)$$

$$V_{E2} = V_{B2} - V_{BE2} \quad (2.40b)$$

For the collector currents

$$I_{C2} \simeq I_{E2} \simeq I_{C1} = \frac{V_{B1} - V_{BE1}}{R_{E1} + R_{E2}} \quad (2.41)$$

The collector voltages are given by

$$V_{C1} = V_{B2} - V_{BE2} \quad (2.42a)$$

$$V_{C2} = V_{CC} - i_{C2}R_C \quad (2.42b)$$

The current through the biasing resistors is given by

$$I_{R1} \simeq I_{R2} \simeq I_{R3} = \frac{V_{CC}}{(R + 1 + R_2 + R_3)} \quad (2.43)$$

and the base currents are given by

$$I_{B1} = I_{C1}/\beta_1 \quad (2.44)$$

$$I_{B2} = I_{C2}/\beta_2 \quad (2.45)$$

2.3.4 Feedback Configured Amplifier

The amplifier of Fig. 2.17(a) used the feedback transistor configuration between transistors Q_1 and Q_2 . Note that the collector of Q_2 feeds back into the emitter of Q_1 . Fig. 2.17(b) is the dc equivalent circuit to be used for analysis. For transistor Q_2 , the base and collector currents are

$$I_{B2} = I_{C1} = \beta_1 I_{B1}, \quad I_{C2} = \beta_2 I_{B2}$$

so that

$$I_{C2} \simeq I_{E2} = \beta_1 \beta_2 I_{B1} \quad (2.46)$$

The collector current I_C is

$$\begin{aligned} I_C = I_{E1} + I_{E2} &\simeq \beta_1 I_{B1} + \beta_1 \beta_2 I_{B1} \\ &= \beta_1 (1 + \beta_2) I_{B1} \end{aligned}$$

$$\Rightarrow I_C \simeq \beta_1 \beta_2 I_{B1} \quad (2.47)$$

We may apply Kirchoff's law from the supply V_{CC} to ground on the input side of the amplifier, Fig. 2.17(b):

$$\begin{aligned} V_{CC} - I_C R_C - V_{EB1} - I_{B1} R_B &= 0 \\ \text{or } V_{CC} - V_{EB1} - \beta_1 \beta_2 I_{B1} R_B &= 0 \end{aligned}$$

so that

$$I_{B1} = \frac{V_{CC} - V_{EB1}}{R_B + \beta_1 \beta_2 R_C} \quad (2.48)$$

The base voltages are

$$V_{B1} = I_{B1} R_B \quad (2.49a)$$

$$V_{B2} = V_{BE2} \quad (2.49b)$$

The collector voltage $V_{C2} = V_{E1}$ and

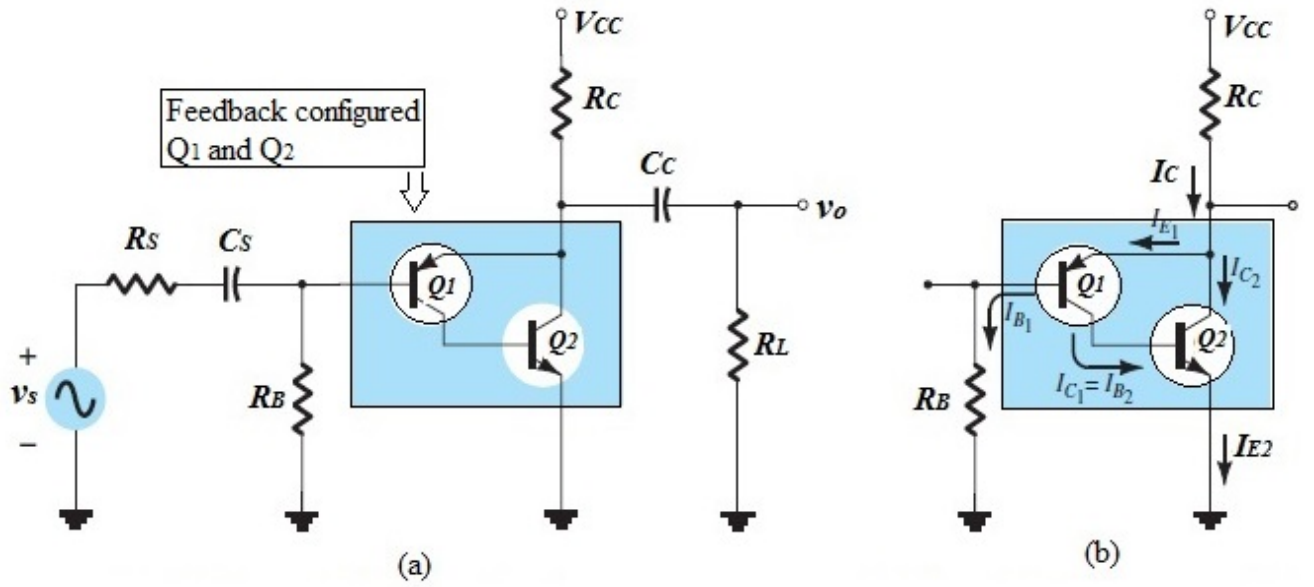


Figure 2.17: Feedback configured amplifier: (a) circuit (b) dc equivalent of (a)

$$V_{C2} = V_{CC} - I_C R_C \quad (2.50a)$$

$$V_{C1} = V_{BE2} \quad (2.50b)$$

For this case,

$$V_{CE2} = V_{C2} \text{ as } E_2 \text{ is grounded} \quad (2.51a)$$

$$V_{EC1} = V_{E1} - V_{C1} \quad (2.51b)$$

$$\Rightarrow V_{EC1} = V_{C2} - V_{BE2} \quad (2.51c)$$

2.3.5 Direct Coupled Amplifier

A Direct Coupled amplifier such is shown in Fig.2.18(a). Note that in comparison with the RC-coupled amplifier of subsection 2.3.1, there is no capacitor between the collector of Q_1 and the base of Q_2 . The purpose of coupling capacitors is to isolate the dc components of each stage. For this amplifier, the dc levels in one stage will directly affect the dc levels in succeeding stages. The benefit is that the coupling capacitor (like C_c in Fig. 2.14(a)) typically limits the low-frequency response of the amplifier. Without coupling capacitors, the amplifier in Fig. 2.18(a) can amplify signals of very low frequency — in fact down to dc. The disadvantage is that any variation in dc levels due to a variety of reasons in one stage can affect the dc levels in the succeeding stages of the amplifier - instability in the operating point. Fig. 2.18(b) is the dc equivalent circuit of Fig. 2.18(a). For Q_1 ,

$$I_{B1} = \frac{E_{Th} - V_{BE}}{R_{Th} + (1 + \beta_1)R_{E1}} \quad (2.52a)$$

$$\text{where } R_{Th} = R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2} \quad (2.52b)$$

$$E_{Th} = \frac{R_2}{R_1 + R_2} V_{CC} \quad (2.52c)$$

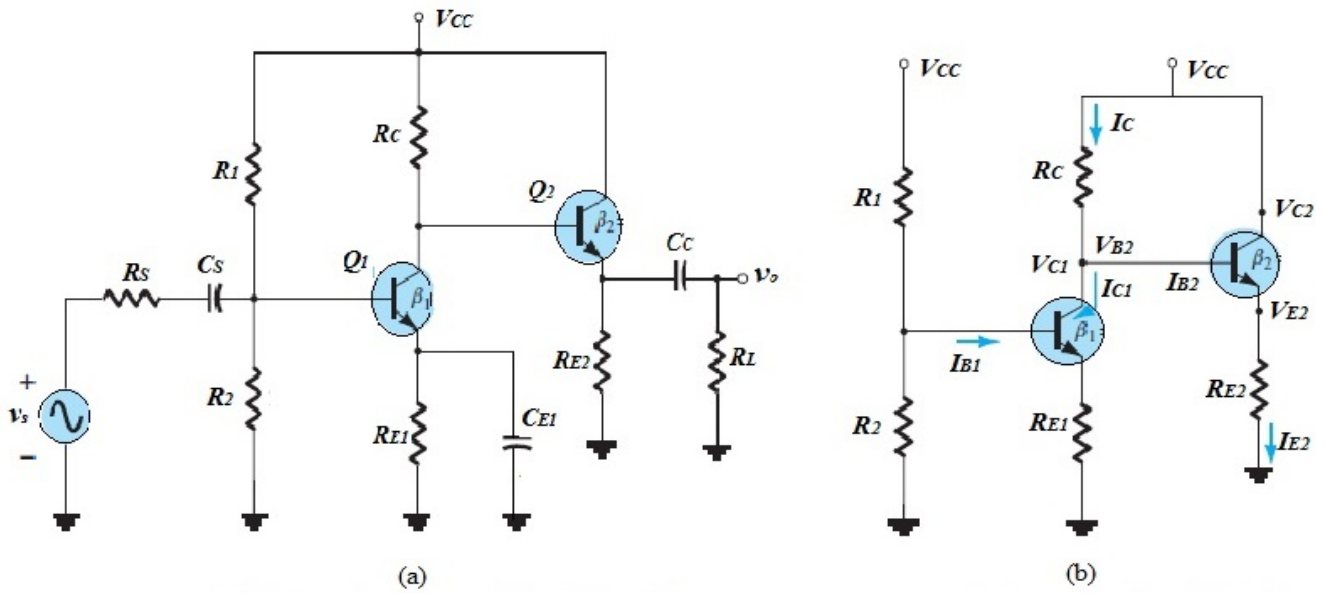


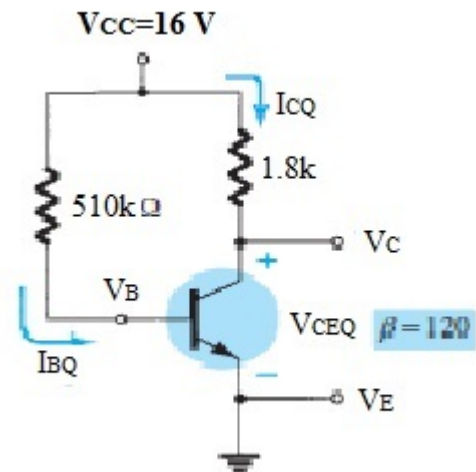
Figure 2.18: (a) Direct-Coupled Amplifier Circuit (b) dc equivalent circuit of (a)

For all configurations use : $V_{BE} \cong 0.7 \text{ V}$ $I_E = (\beta + 1)I_B \cong I_C$ $I_C = \beta I_B$	
#1: Fixed bias:	$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \quad I_C = \beta I_B$
#2: Emitter stabilized:	$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \quad \quad R_i = (\beta + 1)R_E$
#3: Voltage-divider bias:	
(a) Exact:	$R_{Th} = R_1 \parallel R_2 \quad \quad E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} \quad \quad I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$
(b) Approximate: Test if $\beta R_E \geq 10R_2$	
then ...	$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} \quad \quad V_E = V_B - V_{BE} \quad \quad I_E = \frac{V_E}{R_E} \cong I_C$

2.4 Problems

#1: For the fixed bias of the figure, determine:

- (a) I_{BQ} (c) V_{CEQ} (e) V_B
 (b) I_{CQ} (d) V_C (f) V_E



#2: Given the information in the circuit on the right, determine

- (a) I_C (b) R_C
 (c) R_B (d) V_{CE}

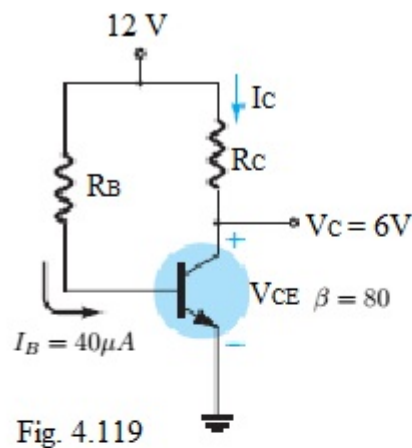


Fig. 4.119

#3: Given the information in Fig. 4.120, determine the following:

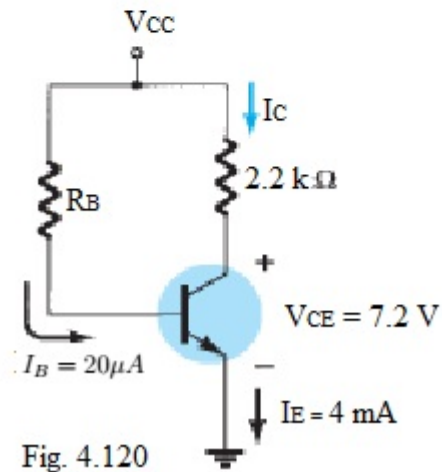


Fig. 4.120

#4: For the emitter-stabilised bias circuit of Fig. 4.122, determine the following:

- (a) I_{BQ} (b) I_{CQ} (c) V_{CEQ}
 (d) V_C (e) V_B (f) V_E

#5: Determine the saturation current (I_{CSAT}) for the circuit of Fig. 4.122

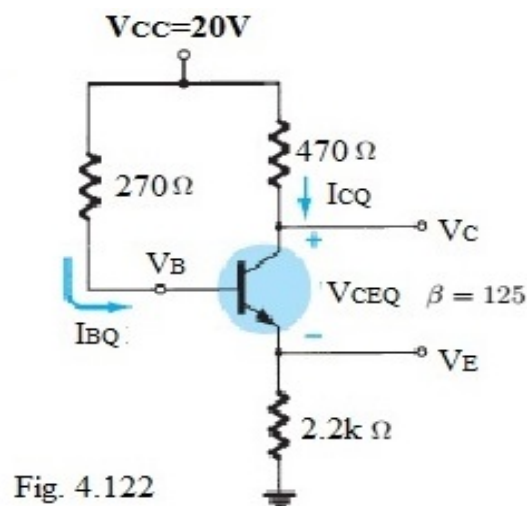


Fig. 4.122

#6: Given the information in Fig. 4.123, determine:

- (a) R_C (b) R_E (c) R_B (d) V_{CE} (e) V_B

#7: For Fig. 4.124, determine

- (a) β (b) V_{CC} (c) R_B

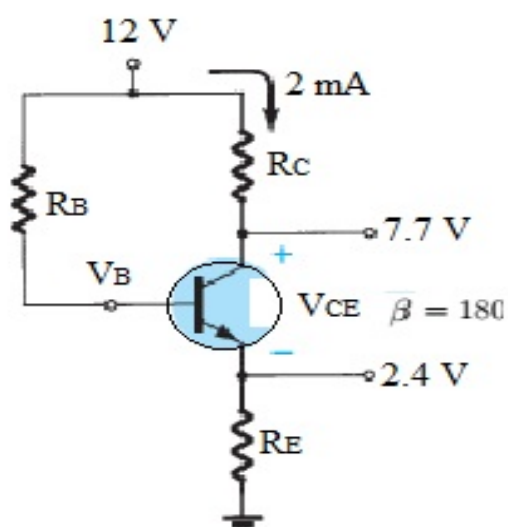


Fig. 4.123

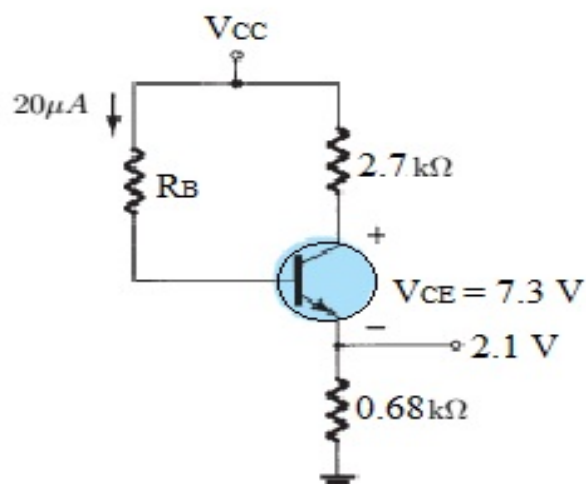


Fig. 4.124

#8: For the voltage-divider bias configuration of Fig. 4.125, determine:

- | | | |
|-------------|--------------|----------|
| a. I_{BQ} | c. V_{CEQ} | e. V_E |
| b. I_{CQ} | d. V_C | f. V_B |

#9: a. Repeat problem #8 for $\beta = 140$ using the general approach (not the approximate).
b. What levels are affected the most? Why?

#10: Given the information provided in Fig. 4.126, determine:

- a. I_C b. V_E c. V_B d. R_1

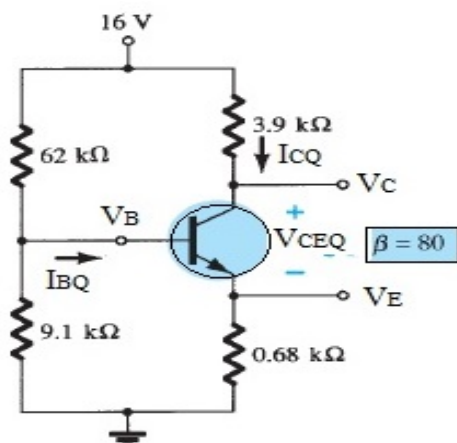


Fig. 4.125

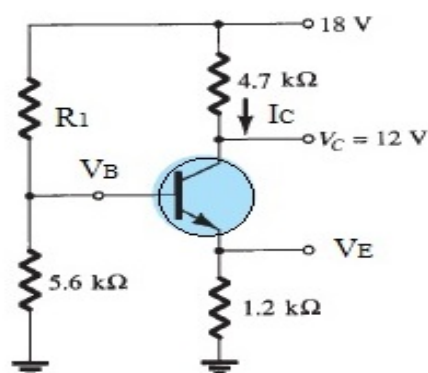


Fig. 4.126

#11: Determine the following for the voltage-divider configuration of Fig. 4.128 using the approximate approach if the condition established is satisfied:

- | | | |
|-------------|----------|----------|
| a. I_C | c. I_B | e. V_B |
| b. V_{CE} | d. V_E | |

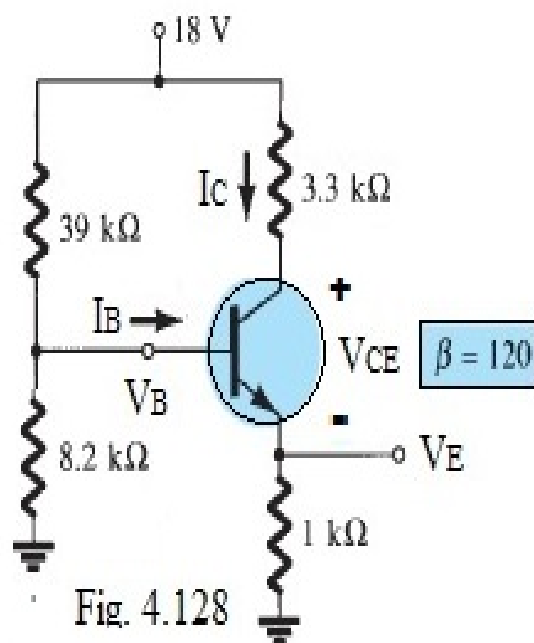


Fig. 4.128